

What is Claimed:

1 2	comprising:	1.	A process for fabricating an electronic device, the process
3		(a.)	forming a first dopant blocking layer at a first temperature; and
4 5	over said first	(b.) dopant	forming a second dopant blocking layer at a second temperature blocking layer.
1 2	lower than sai	2. d secon	A process as recited in claim 1, wherein said first temperature is d temperature.
1 2		3.	A process as recited in claim 1, wherein the process further comprises:
3 4	dopant blocki		g a third dopant blocking layer between said first and said second s.
1 2 3	layer is forme substrate; and		A process as recited in claim 1, wherein said first dopant blocking vertical sidewall of a mesa and over a horizontal surface of a
4		said fin	rst dopant blocking layer has a substantially uniform thickness.
1 2	blocking layer	5. rs are Ir	A process as recited in claim 1, wherein said first and said second nAlAs.
1 2	layer is chose	6. n from t	A process as recited in claim 3, wherein said third dopant blocking the group consisting essentially of InP, InGaP, InGaAs, or InGaAsP
1 2	in the range of	7. f approx	A process as recited in claim 1, wherein said first temperature lies timately 500°C to approximately 570°C.
1 2	range of appro		A process as recited in claim 4, wherein said thickness is in the ly 50 nm to approximately 100 nm.
1 2 3	•		A process as recited in claim 1, wherein said second dopant rertical portion and said vertical portion has a thickness in the range arm to approximately 100 nm.
1 2	dopant blocki	10. ng layer	A process as recited in claim 1, wherein said first and second as are InGaAlAs.



1	11. A process as recited in claim 1, wherein said first dopant blocking layer is disposed above a p-type layer and said second dopant blocking layer is disposed
3	below a semi-insulating layer.
1 2	12. A process a recited in claim 1, wherein said first dopant blocking layer is disposed below a p-type layer and said second dopant blocking layer is disposed
3	above a semi-insulating layer.
1 2 3	13. A process for fabricating an optoelectronic device as recited in claim 1, wherein said second temperature lies in the range of approximately 600° C to approximately 650° C.
1 2	14. A process as recited in claim 1, wherein said first and said second dopant barrier layers are formed by MOVPE.
1 2	15. A process as recited in claim 1, wherein said first and said second dopant barrier layers are formed by MBE.
1 2	16. A process as recited in claim 15, wherein said first temperature lies in the range of approximately 400° C to approximately 470° C.
1 2	17. A process as recited in claim 15, wherein said second temperature lies in the range of approximately 500° C to approximately 550° C.
1 2	18. A process as recited in claim 14, wherein said first temperature is in the range of approximately 500°C to approximately 570°C.
1 2	19. A process as recited in claim 14, wherein said second temperature lies in the range of approximately 600 °C to approximately 650 °C.
1 2	20. A process for fabricating an electronic device, the process comprising:
3	(a.) forming a first InAlAs layer at a first temperature; and
4 5	(b.) forming a second InAlAs layer at a second temperature over said first InAlAs layer.
1 2	21. A process as recited in claim 20, wherein said first temperature is lower than said second temperature.
1	22. A process as recited in claim 20, wherein the process further



3		Iorm	ing a layer of undoped in P between said first and said second in ATA's
4	layers.		
1 2	formed over	23. a vertic	A process as recited in claim 20, wherein said first InAlAs layer is cal sidewall of a mesa and over a horizontal surface of a substrate; and
3		wher	ein said first InAlAs layer has a substantially uniform thickness.
1 2 3	disposed abo	-	A process as recited in claim 20, wherein said first InAlAs layer is type layer and said second InAlAs layer is disposed below a semi-
1 2 3	disposed beloinsulating lay	-	A process a recited in claim 20, wherein said first InAlAs layer is type layer and said second InAlAs layer is disposed above a semi-
1 2 3	20, wherein approximate		A process for fabricating an electronic device as recited in claim cond temperature lies in the range of approximately 600 °C to °C.
1 2	in the range	27. of appro	A process as recited in claim 20, wherein said first temperature lies eximately 500 °C to approximately 570 °C.
1 2	dopant block	28. ting laye	A process as recited in claim 20, wherein said first and said second ers are formed by MOVPE.
1 2	in the range	29. of appro	A process as recited in claim 20, wherein said first temperature lies eximately 400 °C to approximately 470 °C.
1 2	lies in the rai	30. nge of a	A process as recited in claim 20, wherein said second temperature approximately 500° C to approximately 550° C.
1 2	dopant block	31. sing laye	A process as recited in claim 20 wherein said first and said second ers are formed by MBE.
1		32.	An electronic device, comprising:
2	second dope		ltilayer dopant barrier disposed between a first doped layer and a said multilayer dopant barrier further comprising:
4		a firs	t dopant blocking layer disposed adjacent said first doped layer; and
5		a sec	ond donant blocking layer disposed adjacent said second doned layer

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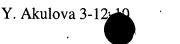
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33.	An electronic device as recited in claim 32, wherein said first
doped layer is	s in a mesa, and said second doped layer disposed on at least one side
of said mesa.	
34	An electronic device as recited in claim 33, wherein said first

- dopant blocking layer has a vertical portion adjacent a vertical sidewall of said mesa and a horizontal portion above a substrate.
- 35. An electronic device as recited in claim 32, wherein said first dopant blocking layer substantially prevents dopants from diffusing out of said first doped layer.
- 36. An electronic device as recited in claim 32, wherein said second dopant blocking layer substantially blocks dopants from diffusing out of said second doped layer.
- 37. An electronic device as recited in claim 32, wherein said first dopant blocking layer is InAlAs.
- 38. An electronic device as recited in claim 32, wherein said second dopant blocking layer is InAlAs.
- 39. An electronic device as recited in claim 34, wherein said vertical portion and said horizontal portion have a substantially identical thickness.
- 40. An electronic device as recited in claim 32, wherein said first dopant blocking layer has a resistivity in the range of approximately $10^6 \Omega$ —cm to approximately $10^9 \Omega$ -cm.
- 41. An electronic device as recited in claim 32, wherein said second dopant blocking layer has a resistivity in the range of approximately $10^4 \Omega$ -cm to $10^5 \Omega$ cm.
- 42. An electronic device as recited in claim 32, wherein said first doped layer is p-doped InP and said second doped layer is InP(Fe).
- An electronic device as recited in claim 32, wherein said first 1 43. 2 dopant blocking layer substantially blocks Zn dopants and said second dopant blocking 3 layer substantially blocks iron dopants.
- 1 44. An electronic device as recited in claim 32, wherein the electronic device is chosen from the group consisting essentially of light emitting and light detecting 2 3 optoelectronic devices.



1 2	45. An electronic device as recited in claim 32, wherein said first and said second dopant blocking layers are InAlGaAs.
1 2	46. An electronic device as recited in claim 32, wherein said multi-layer dopant barrier further comprises:
3 4	a third dopant blocking layer disposed between said first and said second dopant blocking layers.
1 2 3	47. An electronic device as recited in claim 46, wherein said third dopant blocking layer is chosen from the group consisting essentially of InP, InGaP, InGaAs and InGaAsP.
1	48. An electronic device, comprising:
2 3	a multilayer dopant barrier disposed between a first doped layer and a second doped layer, said multilayer dopant barrier further comprising:
4	a first dopant blocking layer contiguous with said first doped layer; and
5	a second dopant blocking layer contiguous with said second doped layer.
1 2 3	49. An electronic device as recited in claim 48, wherein said first doped layer is in a mesa, and said second doped layer is disposed on at least one side of said mesa.
1 2 3	50. An electronic device as recited in claim 49, wherein said first dopant blocking layer has a vertical portion adjacent a vertical sidewall of said mesa and a horizontal portion above a substrate.
1 2 3	51. An electronic device as recited in claim 48, wherein said first dopant blocking layer substantially prevents dopants from diffusing out of said first doped layer.
1 2 3	52. An electronic device as recited in claim 48, wherein said second dopant blocking layer substantially blocks dopants from diffusing out of said second doped layer.
1	53. An electronic device as recited in claim 48, wherein said first and
2	said second dopant blocking layers are InAlAs.
1 2	54. An electronic device as recited in claim 48, wherein said multi-layer dopant barrier further comprises:



3	a third dopant blocking layer disposed between said first and said second
4	dopant blocking layers.
1	55. An electronic device as recited in claim 54, wherein said third
2	dopant blocking layer is chosen from the group consisting essentially of InP,
3	InGaP, InGaAs and InGaAsP.
1	56. An electronic device as recited in claim 48, wherein said first
2	doped layer is p-type and said second doped layer is semi-insulating.
1	57. An electronic device as recited in claim 48, wherein said first and
2	said second dopant blocking layers are InAlGaAs.
1	58. An electronic device as recited in claim 48, the electronic device is
2	chosen from the group consisting essentially of light emitting and light detecting
3	optoelectronic devices.

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